IN THE CLAIMS:

Claims 18, 21-23, and 26-28 have been amended as follows and claim 20 has been canceled, without prejudice. The current state of the pending claims is listed below:

1-17. (Previously Canceled).

18. (Currently Amended) An integrated circuit arrangement, comprising:

~~at least one module including one of an individual module and a plurality of ordered modules~~ a plurality of modules, each ~~module of the at least one module~~ of the modules having at least one input and at least one output, ~~the at least one module~~ each of the modules forming at least one cell, the at least one cell including at least one of a bus system, an arithmetic and logic unit and a configurable logic cell;

a supplementary module assigned to at least one of the modules ~~the at least one module and being of a same kind as the at least one module~~;

~~a first switching element coupled to the at least one input of a particular module and being upstream from the at least one input of the particular module, the first switching element switching an input signal to at least one of the particular module and a module following the particular module; and~~

~~a second switching element coupled to the at least one output of the particular module and being downstream from the at least one output of the particular module;~~

~~wherein, if an error occurs in a module, then at least one of a defective module and a defective function cell is replaced by a module following the at least one of the defective module and the defective function cell by switching the first switching element and by switching the second switching element, a last module being replaced by the supplementary module;~~

at least one input multiplexer coupled upstream to the inputs of the modules, each of the at least one input multiplexers configured to switch, in each case, an input signal between one a first one of the modules and a second one of the modules;

at least one output multiplexer coupled downstream from the outputs of the modules, the at least one output multiplexer configured to switchably receive, in each case, an output signal of the first one of the modules and an output signal of the second one of the modules; and

a control configured to control the at least one input multiplexer and the at least one output multiplexer to exclude a defective one of the modules, the control using a single decoder to perform at least one of (A) switching all of the at least one input multiplexer and the at least one output multiplexer in the same direction, and (B) switching all of the at least one input multiplexer and the at least one output multiplexer so that two groups of consecutive multiplexers are formed, multiplexers within each of the groups being switched in the same direction, the two groups being switched in different directions, the control performing the switching so that the defective one of the module is excluded .

19. (Previously Presented) The integrated circuit arrangement according to claim 18, wherein the error is detected via self-testing.

20. (Currently Canceled) The integrated circuit arrangement according to claim 18, further comprising:

a control that controls the first switching element and the second switching element, at least one of (A) the control switching all of the switching elements in the same way and (B) all of the switching elements forming a first group of switching elements and a second group of switching elements, the control switching all of the switching elements in the first group in a first way and switching all of the switching elements in the second group in a second way, the first group and the second group being switched differently to exclude the defective module from the switching elements.

21. (Currently Amended) The integrated circuit arrangement according to claim ~~20~~ 18, wherein the control is ~~adapted~~ configured to decode a binary value so as to yield at least one of the first group and the second group.

22. (Currently Amended) The integrated circuit arrangement according to claim ~~20~~ 18, wherein the control is ~~adapted~~ configured to encode a binary value, the binary value defining at least one of a switching element group and a switching element circuit.

23. (Currently Amended) ~~The integrated circuit arrangement according to claim 22~~ An integrated circuit arrangement, comprising:

at least one module including one of an individual module and a plurality of ordered modules, each module of the at least one module having at least one input and at least one output, the at least one module forming at least one cell, the at least one cell including at least one of a bus system, an arithmetic and logic unit and a configurable logic cell;

a supplementary module assigned to the at least one module and being of a same kind as the at least one module;

a first switching element coupled to the at least one input of a particular module and being upstream from the at least one input of the particular module, the first switching element switching an input signal to at least one of the particular module and a module following the particular module; and

a second switching element coupled to the at least one output of the particular module and being downstream from the at least one output of the particular module,

wherein , if an error occurs in a module, then at least one of a defective module and a defective function cell is replaced by a module following the at least one of the defective module and the defective function cell by switching the first switching element and by switching the second switching element, a last module being replaced by the supplementary module, and wherein the binary value is generated by a counter.

24. (Previously Presented) The integrated circuit arrangement according to claim ~~22~~, wherein the binary value is provided via a look-up-table arrangement.

25. (Previously Presented) The integrated circuit arrangement according to claim ~~18~~, further comprising:

a memory that stores a binary value, the binary value indicating at least

one of the defective module and all defective modules.

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26. (Currently Amended) ~~The integrated circuit arrangement according to claim 25~~ An integrated circuit arrangement, comprising:

at least one module including one of an individual module and a plurality of ordered modules, each module of the at least one module having at least one input and at least one output, the at least one module forming at least one cell, the at least one cell including at least one of a bus system, an arithmetic and logic unit and a configurable logic cell;

a supplementary module assigned to the at least one module and being of a same kind as the at least one module;

a first switching element coupled to the at least one input of a particular module and being upstream from the at least one input of the particular module, the first switching element switching an input signal to at least one of the particular module and a module following the particular module;

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a second switching element coupled to the at least one output of the particular module and being downstream from the at least one output of the particular module; and

a memory that stores a binary value, the binary value indicating at least one of the defective module and all defective modules;

wherein , if an error occurs in a module, then at least one of a defective module and a defective function cell is replaced by a module following the at least one of the defective module and the defective function cell by switching the first switching element and by switching the second switching element, a last module being replaced by the supplementary module, and wherein the memory that stores a binary value is independent of a system start.

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27. (Currently Amended) A method for testing an integrated circuit having cells, comprising the steps of:

testing a cell function of the integrated circuit by executing, with the cells, a test program including calculating test vectors;

performing, with at least one of the cells wired as a comparator, a comparison between a test result and a setpoint result; and

indicating an error if the comparison indicates a deviation between the setpoint result and the test result so that, in response to the error, a module having the cell found to be defective is replaced.

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28. (Currently Amended) ~~The method according to claim 27~~ A method for testing an integrated circuit having cells, comprising the steps of:

testing a cell function of the integrated circuit by executing, with the cells, a test program including calculating test vectors;

performing, with at least one of the cells, a comparison between a test result and a setpoint result; and

indicating an error if the comparison indicates a deviation between the setpoint result and the test result so that, in response to the error, a module having the cell found to be defective is replaced;

wherein the step of testing the cell function includes the step of testing a cell array by at least one of exchanging and mirroring a test algorithm that includes a plurality of calculations at least once within the cell array.

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29. (Previously Presented) The method according to claim 27, wherein the step of testing the cell function includes the step of calling up test data from an integrated memory in the integrated circuit, the test data being used for executing the test program.

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30. (Previously Presented) The method according to claim 27, wherein the method for testing the integrated circuit is carried out at a system start.

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31. (Previously Presented) The method according to claim 27, wherein the method for testing the integrated circuit is carried out as a self-test method of application programs running during at least one of a wait cycle and an IDLE cycle.

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32. (Previously Presented) The method according to claim 31, wherein the self-test method is at least one of called up from an application program and integrated into an application program.

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33. (Previously Presented) The method according to claim 27, further comprising the

steps of:

saving data from arithmetic and logic units to a chip-internal memory before running a test algorithm; and

loading data back into the arithmetic and logic units after running the test algorithm.

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34. (Previously Presented) The method according to claim 33, further comprising the steps of:

shutting down registers in the arithmetic and logic units before running the test algorithm;

using test registers for the test algorithms; and

connecting the registers in the arithmetic and logic units after running the test algorithm.

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35. (Previously Presented) The method according to claim 27, further comprising the steps of:

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assigning at least one additional supplementary module to a number of ordered modules forming the cells, the at least one additional supplementary module and the ordered modules being of the same kind, each module having at least one input and at least one output;

coupling a first switching element to the at least one input of a particular module, the first switching element being disposed upstream from the at least one input of the particular module, the first switching element being ~~adapted~~ configured to switch an input signal to one of the particular module and a module following the particular module;

coupling a second switching element to the at least one output of the particular module, the second switching element being disposed downstream from the at least one output of the particular module, the second switching element being ~~adapted~~ configured to receive an output from one of the particular module and the module following the particular module; and

if an error is detected in a module, then replacing a defective module by a module following the defective module by switching the first switching element and the second switching element, a last module in the ordered modules

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being replaced by the supplementary module.

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